



MODULE DESCRIPTION

Module code	
Module name	Architektura systemów komputerowych 1
Module name in English	Computer Systems Architecture 1
Valid from academic year	2012/13

MODULE PLACEMENT IN THE SYLLABUS

Subject	Computer Science
Level of education	1st degree <i>(1st degree / 2nd degree)</i>
Studies profile	General <i>(general / practical)</i>
Form and method of conducting classes	Full-time <i>(full-time / part-time)</i>
Specialisation	
Unit conducting the module	The Department of Computer Science
Module co-ordinator	Prof. Krzysztof Sapiecha, PhD hab., Eng.
Approved by:	

MODULE OVERVIEW

Type of subject/group of subjects	Major <i>(basic / major / specialist subject / conjoint / other HES)</i>
Module status	Compulsory <i>(compulsory / non-compulsory)</i>
Language of conducting classes	Polish
Module placement in the syllabus - semester	2nd semester
Subject realisation in the academic year	Summer semester <i>(winter / summer)</i>
Initial requirements	Arithmetic and Logic Systems <i>(module codes / module names)</i>
Examination	Yes <i>(yes / no)</i>
Number of ECTS credit points	5

Method of conducting classes	Lecture	Classes	Laboratory	Project	Other
Per semester	30		30		



TEACHING RESULTS AND THE METHODS OF ASSESSING TEACHING RESULTS

Module target	The aim of the module is to familiarise students with the structure and functioning methods of a modern computer and microprocessor. Another aim is to discuss microprocessor architecture, memory, and present the interaction of these devices. Finally, the aim of the module is to present various designing aspects concerning a microprocessor as well as a complete computer system (together with their utilisation methods).
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Effect symbol	Teaching results	Teaching methods (l/c/l/p/other)	Reference to subject effects	Reference to effects of a field of study
W_01	Knowledge of a modular microprocessor structure and microprocessor architecture (von Neumann and Harvard). Knowledge of microprocessor interaction, memory, and in-out devices. Knowledge of interrupts, buses, and DMA. Knowledge as regards designing microprocessors.	I	K_W08	T1A_W02
W_02	Knowledge of the structure of a modern computer. Vast knowledge as regards the issues connected with microprocessors, memories, and devices to build a computer.	I	K_W08 K_W18 K_W20	T1A_W05 T1A_W06
W_03	Knowledge concerning the fundamentals of programming in a machine language (assembler).	I	K_W08	T1A_W02
W_04	Vast knowledge as regards the following: the application of memory, memory structures, and various notions connected with computer memory.	I	K_W18	T1A_W05
W_05	Knowledge of modern solutions applied in microprocessors.	I	K_W08	T1A_W02
U_01	The ability to design a microprocessor.	I	K_U01 K_U03 K_U14	T1A_U01 T1A_U07 T1A_U03 T1A_U09 T1A_U14 T1A_U16
K_01	Teamwork.	I	K_U02	T1A_U02

Teaching contents:

Teaching contents as regards lectures

Lecture number	Teaching contents	Reference to teaching results for a module
1	Computers – their structure and principles of operation.	W_02
2	The structure and principles of operation of a microprocessor.	W_01
3	Memory, internal computer devices, and attachment.	W_01, W_02, W_04
4	Microprocessor designing – instruction set.	W_01
5	Microprocessor designing – an arithmetic logic unit.	W_01
6	Buses – basic messages, the issue of arbitrage, and work cycles of buses.	W_01
7	Microprocessor designing – the design of a datapath and controlling unit for single-cycle instructions.	W_01



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8	Microprocessor designing – the design of a datapath and controlling unit for multi-cycle instructions.	W_01
9	Memory – basic messages, cache memory, and virtual memory.	W_04, W_02
10	Microprocessor designing – a co-operation with memory.	W_01, W_04
11	In/out devices, interruptions, and DMA.	W_01, W_04
12	Microprocessor designing – co-operation with in/out devices.	W_01, W_02
13	Microprocessor designing – implementation techniques.	W_01
14	Microprocessor designing in a machine language.	W_03
15	The directions of development concerning microprocessor architectures.	W_05

Teaching contents as regards laboratory classes

Laboratory class number	Teaching contents	Reference to teaching results for a module
1	Discussing a PC class computer structure.	W_02
2	Completing tasks which consist in starting a debugger checking microprocessor operating methods – arithmetic and logic instructions.	W_03
3	Familiarising students with the Quartus environment, completing tasks presenting the utilisation of microprocessor designing modules.	W_01
4	Completing a microprocessor design – preparing construction assumptions, an order list design, and an order design.	W_01
5	Completing an arithmetic logic unit (ALU).	W_01
6	Completing assumptions prepared during laboratory classes No 4 with interruptions, a DMA controller, and an internal bus controller of a microprocessor.	W_01
7	Completing a datapath and a control unit for single-cycle orders.	W_01
8	Completing a design of a memory controller, taking the assumptions prepared during laboratory class No 4 into consideration.	W_01, W_04
9	Selecting construction assumptions of a microprocessor – allocating a project assignment for a student's individual completion (based on the knowledge acquired during laboratory classes No 3-8). Preparing a solution according to knowledge acquired during laboratory class No 4.	U_01, K_01
10	A student's independent task completion allocated during laboratory class No 9 – completing activities in compliance with the knowledge acquired during laboratory class No 5.	U_01, K_01
11	A student's independent task completion allocated during laboratory class No 9 – completing activities in compliance with the knowledge acquired during laboratory class No 6.	U_01, K_01
12	A student's independent task completion allocated during laboratory class No 9 – completing activities in compliance with the knowledge acquired during laboratory class No 7.	U_01, K_01
13	A student's independent task completion allocated during laboratory class No 9 – completing activities in compliance with the knowledge acquired during laboratory class No 8.	U_01, K_01
14	A student's independent task completion allocated during laboratory class No 9 – completing a program testing a microprocessor in its machine code.	U_01, K_01
15	Project presentation prepared during laboratory classes No 9-14.	U_01

The methods of assessing teaching results

Effect symbol	Methods of assessing teaching results <i>(assessment method, including skills – reference to a particular project, laboratory assignments, etc.)</i>



W_01	An examination
W_02	An examination
W_03	An examination
W_04	An examination
W_05	An examination
U_01	Obtaining a credit for laboratory classes based on initial tests, reports from the completed assignments and a report from completing a project assignment during laboratory classes.

STUDENT'S INPUT

ECTS credit points		
	Type of student's activity	Student's workload
1	Participation in lectures	30
2	Participation in classes	
3	Participation in laboratories	30
4	Participation in tutorials (2-3 times per semester)	3
5	Participation in project classes	
6	Project tutorials	
7	Participation in an examination	2
8		
9	Number of hours requiring a lecturer's assistance	65 <i>(sum)</i>
10	Number of ECTS credit points which are allocated for assisted work <i>(1 ECTS credit point=25-30 hours)</i>	3
11	Unassisted study of lecture subjects	15
12	Unassisted preparation for classes	
13	Unassisted preparation for tests	
14	Unassisted preparation for laboratories	15
15	Preparing reports	4
16	Preparing for a final laboratory test	
17	Preparing a project or documentation	4
18	Preparing for an examination	30
19	Preparing questionnaires	
20	Number of hours of a student's unassisted work	68 <i>(sum)</i>
21	Number of ECTS credit points which a student receives for unassisted work <i>(1 ECTS credit point=25-30 hours)</i>	2
22	Total number of hours of a student's work	133
23	ECTS credit points per module <i>1 ECTS credit point=25-30 hours</i>	5
24	Work input connected with practical classes <i>Total number of hours connected with practical classes</i>	14
25	Number of ECTS credit points which a student receives for practical classes <i>(1 ECTS credit point=25-30 hours)</i>	0.5