



Projekt współfinansowany ze środków Unii Europejskiej w ramach Europejskiego Funduszu Społecznego

MODULE DESCRIPTION

Module code	
Module name	Architektura systemów komputerowych 2
Module name in English	Computer Systems Architecture 2
Valid from academic year	2012/13

MODULE PLACEMENT IN THE SYLLABUS

Subject	Computer Science
Level of education	1st degree (1st degree / 2nd degree)
Studies profile	General (general / practical)
Form and method of conducting classes	Full-time (full-time / part-time)
Specialisation	
Unit conducting the module	The Department of Computer Science
Module co-ordinator	Roman Stanisław Deniziak, PhD hab., Eng., Professor of the University
Approved by:	

MODULE OVERVIEW

Type of subject/group of subjects	Major (basic / major / specialist subject / conjoint / other HES)
Module status	Compulsory (compulsory / non-compulsory)
Language of conducting classes	Polish
Module placement in the syllabus - semester	3rd semester
Subject realisation in the academic year	Winter semester (winter / summer)
Initial requirements	Arithmetic and Logic Systems, Computer Systems Architecture 1 (module codes / module names)
Examination	Yes (yes / no)
Number of ECTS credit points	5

Method of conducting classes	Lecture	Classes	Laboratory	Project	Other
Per semester	30			15	



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TEACHING RESULTS AND THE METHODS OF ASSESSING TEACHING RESULTS

Module target	The aim of the module is to familiarise students with: the structure of modern RISC processors, superscalar and multi-core processors, as well as with the principles of pipelining and parallel processing. Another aim is to acquaint students with the ability to design microprogrammed control.
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Effect symbol	Teaching results	Teaching methods (I/c/l/p/other)	Reference to subject effects	Reference to effects of a field of study
W_01	Knowledge of the structure and operation as regards RISC, superscalar, and multithreaded processors.	I	K_W08	T1A_W03
W_02	Knowledge of parallel computer architecture.	I	K_W08	T1A_W03
W_03	Knowledge of the structures and designing principles of microprogrammed control units.	I	K_W08	T1A_W04 T1A_W07
W_04	Knowledge of the directions of development as regards computer systems architecture.	I	K_W18	T1A_W05
U_01	The ability to design microprogrammed control units.	p	K_U02 K_U03 K_U14	T1A_U02 T1A_U03 T1A_U09 T1A_U14 T1A_U16
K_01	Teamwork.	p	K_K03	T1A_K03

Teaching contents:

Teaching contents as regards lectures

Lecture number	Teaching contents	Reference to teaching results for a module
1	The directions of development concerning computer systems architecture.	W_04
2	The structure and operation of the microprogrammed control unit.	W_03, U_01
3	The methods of ordering microorders.	W_03, U_01
4	A microprogrammed control unit (controlling a processor).	W_03, U_01
5	Techniques applied in dual-core processors.	W_04
6	The principles of pipelining.	W_01
7	Optimisation methods as regards pipeline order execution. Hop forecasting.	W_01
8	RISC processors.	W_01
9	Optimisation methods of carrying out programs in RISC processors.	W_01
10	Superscalar processors.	W_01
11	Parallel architectures, Flynn's classification, and vector processes.	W_02
12	SMP architectures.	W_02
13	Cluster architectures, CCNUMA, and COMA.	W_02
14	Hardware support of an operating system.	W_04
15	The architectures of modern supercomputers.	W_02 W_04

The characteristics of project assignments

The subject matter covers designing a microprogrammed control unit for the processor with the assigned internal structure and order list. As part of the project, a student ought to:

- design order formats
- design a microprogram in a symbolic form



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- design the structure of a microprogrammed control unit
- encrypt microorders and distribute them in microprogram memory
- implement a processor using ready-made modules using Quartus II design environment, prepare a testing program, and make a simulation verifying the correctness of executing all orders

The methods of assessing teaching results

Effect symbol	Methods of assessing teaching results <i>(assessment method, including skills – reference to a particular project, laboratory assignments, etc.)</i>
W_01	An examination
W_02	An examination
W_03	An examination
W_04	An examination
U_01	Obtaining a credit for the project on the basis of a report

STUDENT'S INPUT

ECTS credit points		
	Type of student's activity	Student's workload
1	Participation in lectures	30
2	Participation in classes	
3	Participation in laboratories	
4	Participation in tutorials (2-3 times per semester)	3
5	Participation in project classes	15
6	Project tutorials	15
7	Participation in an examination	2
8		
9	Number of hours requiring a lecturer's assistance	65 <i>(sum)</i>
10	Number of ECTS credit points which are allocated for assisted work <i>(1 ECTS credit point=25-30 hours)</i>	3
11	Unassisted study of lecture subjects	15
12	Unassisted preparation for classes	
13	Unassisted preparation for tests	
14	Unassisted preparation for laboratories	
15	Preparing reports	
16	Preparing for a final laboratory test	
17	Preparing a project or documentation	15
18	Preparing for an examination	30
19	Preparing questionnaires	
20	Number of hours of a student's unassisted work	60 <i>(sum)</i>
21	Number of ECTS credit points which a student receives for unassisted work <i>(1 ECTS credit point=25-30 hours)</i>	2
22	Total number of hours of a student's work	125
23	ECTS credit points per module <i>1 ECTS credit point=25-30 hours</i>	5



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24	Work input connected with practical classes <i>Total number of hours connected with practical classes</i>	45
25	Number of ECTS credit points which a student receives for practical classes <i>(1 ECTS credit point=25-30 hours)</i>	2